

REMARKS

In response to the Office Action mailed September 9, 2004, Applicants respectfully request reconsideration.

As a preliminary matter, Applicants note with appreciation the indication of allowable subject matter in claims 2-6.

Claim 1 was rejection under 35 U.S.C. §102(b) as being anticipated by Gens et al. Applicants respectfully traverse this rejection. Figure 3 of Gens, referred to in the Office Action shows a P-channel MOS transistors M10L and M10R serially connected. The output of the series connection is provided at terminal S, which is connected to the midpoint of the serial connection of transistors M10L and M10R.

By contrast, claim 1 recites a linear regulator having an output stage comprising first and second P-channel MOS transistors serially connected between a first D.C. supply terminal and an output terminal providing a regulated output voltage, and a circuit for controlling the first and second transistors capable of providing said first and second transistors with first and second control signals as a function of the output voltage and the voltage at the midpoint of the series connection. Gens does not teach or suggest P-channel MOS transistors serially connected between a first D.C. supply terminal and an output terminal to provide a regulated output voltage. As noted, the output of Gens is provided at the midpoint of the serial connection of the transistors. Accordingly, claim 1 distinguishes over Gens and is in allowable condition. Accordingly, withdrawal of the rejection under 35 U.S.C. §102(b) is respectfully requested.

Claim 1 was also rejected under 35 U.S.C. §103(a) as being unpatentable over Ferry in view of Gens. Applicants respectfully traverse this rejection.

First, since Gens illustrates an output terminal taken at the midpoint of the serial connection of transistors M10L and M10R, any such combination between Gens and Ferry is improper.

Furthermore, Ferry, like Gens, illustrates an output terminal S that is also disposed at the midpoint of the serial connection of MOS transistors MP and MN. Therefore, one skilled in the art would not be motivated to combine Gens and Ferry as described in the Office Action.

Furthermore, claim 1 still distinguishes over any such combination of Gens and Ferry because

Gens or Ferry , either taken alone or in combination, do not teach or suggest at least first and second P-channel MOS transistors serially connected between a first D.C. supply terminal and an output terminal to provide a regulated output voltage. Accordingly, claim 1 distinguishes over Gens or Ferry alone or in combination and is in allowable condition. Withdrawal of the rejection of claim 1 under 35 U.S.C. §103(a) is respectfully requested.

Claims 2-6 depend from claim 1 and are allowable for at least the same reasons.

Applicants have also added claims 7-12 to the application. Claim 7 is an independent claim with claims 8-12 depending therefrom. Claim 7 recites a linear regulator having an output stage comprising first and second P-channel MOS transistors serially connected between a first terminal and an output terminal to provide a regulated output voltage, and a circuit that controls the first and second transistors capable of providing said first and second transistors with first and second control signals as a function of the output voltage and the voltage at the midpoint of the series connection. Clearly, none of the references of record teach or suggest the limitations of claim 7.

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CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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